In the Claims:

Please renumber the misnumbered first instance of claim 12 to claim 11. Please amend claims 1-4, 6, 7, 10, 11, 14-16 and 20. Please add new claims 21-26. . The claims are as follows:

1. (Currently Amended) A method of testing and repairing an integrated circuit chip having a total number of fuses for effecting repair of said integrated circuit, comprising:

~~testing a memory array with a set of tests and~~ reserving a first number of said total number of fuses for use in repairing said memory array based on results of ~~said~~ a set of standard memory tests; ~~and~~

performing said set of standard memory tests; and

shmoo memory testing said memory array by incrementing, decrementing, or both incrementing and decrementing values of a test parameter until a predetermined minimum or a predetermined maximum value of said test parameter is reached and that ~~utilizes a~~ requires no more than a second number of said total number of fuses for use in repairing said memory array to operate at said predetermined minimum or said predetermined maximum value of said test parameter.

2. (Currently Amended) The method of claim 1, wherein (i) said first number of fuses plus said second number of fuses equals said total number of fuses or (ii) said first number of fuses plus said second number of fuses ~~equal said total number of fuses minus~~ plus a ~~predetermined~~ third number of fuses equals said total number of fuses.

3. (Currently Amended) The method of claim 1, further including:

collecting fuse data based on said standard memory testing ~~a memory array with a set of tests~~; and

collecting fuse data based on said shmoo memory testing.

4. (Currently Amended) The method of claim 3, further including:

programming said fuses to effect repair of said memory array based on said fuse data based on said standard memory testing ~~said memory array with said set of tests~~ and based on said fuse data based on said shmoo memory testing.

5. (Original) The method of claim 1, wherein said test parameter is the minimum specified operating voltage of said memory array.

6. (Currently Amended) The method of claim 1, further including:

repairing said memory array based on results of said ~~first set of tests~~ standard memory testing by replacement of one or more wordlines in said memory array with one or more redundant wordlines; and

repairing said memory array to operate at said minimum or maximum value of said test parameter of said shmoo memory testing by replacement of one or more wordlines in said memory array with one or more redundant wordlines.

7. (Currently Amended) The method of claim 1, wherein said incrementing, decrementing or incrementing and decrementing values of [[a]] said test parameter until a minimum or maximum value of said test parameter is reached comprises a ~~linear or~~ binary process.

8. (Original) The method of claim 1, wherein said memory array comprises static random access memory cells or dynamic random access memory cells.

9. (Original) The method of claim 1, wherein said memory array is an embedded memory array.

10. (Currently Amended) A method of testing and repairing [[an]] integrated circuit chips having a total number of fuses for effecting repair of said integrated circuit, comprising:

(a) selecting an integrated circuit chip on a wafer for testing;

(b) selecting a test parameter for shmoo memory testing;

(c) reserving a first number of said total number of fuses for use in repairing said memory array based on results of said set of tests and then testing a memory array on said selected integrated circuit chip with a set of standard memory tests and ~~reserving a first number of said total number of fuses for use in repairing said memory array based on results of said set of tests~~;

(d), shmoo memory testing said memory array by incrementing, decrementing, or both incrementing and decrementing values of a test parameter until (i) a predetermined minimum or a predetermined maximum value of said test parameter is reached and that ~~utilizes a~~ requires no more than a second number of said total number of fuses for use in repairing said memory array to operate at said predetermined minimum or said predetermined maximum value of said test parameter;

(e) saving a first set of fuse data based on said standard memory testing of said memory array ~~on said selected integrated circuit with said set of tests~~ and saving a second set of fuse data based on said shmoo memory testing of said memory array; and

(f) repeating steps (a) through (e) until all integrated circuit chips to be tested have been selected.

[[12]] 11. (Currently Amended) The method of claim 10, wherein (i) said first number of fuses plus said second number of fuses equals said total number of fuses or (ii) said first number of fuses plus said second number of fuses ~~equal said total number of fuses minus~~ plus a ~~predetermined~~ third number of fuses equals said total number of fuses.

12. (Original) The method of claim 10, wherein a number of times said test parameter is incremented or decremented is limited to a predetermined number of times even if said minimum or maximum value of said test parameter is not reached.

13. (Currently Amended) The method of claim 10, further including:

(g) programming said total number of fuses to effect repair of said memory array based on said first set of fuse data based ~~on said testing said memory array with said set of tests~~ and based on said second set of fuse data ~~based on said shmoo testing said memory array~~.

14. (Currently Amended) The method of claim 10, further including:

between steps (c) and (d), programming said fuses to effect repair of said memory array based on said first set of fuse data ~~based on said testing said memory array with said set of tests~~; and

after step (d), programming said fuses to effect repair of said memory array based on said second set of fuse data ~~based on said shmoo testing said memory array~~.

15. (Currently Amended) The method of claim 10 further including:

(g) repairing said memory array based on results of said ~~first set of tests~~ standard memory testing by replacement of wordlines in said memory array with redundant wordlines; and

(h) repairing said memory array to operate at said minimum or at said maximum value of said test parameter by replacement of wordlines in said memory array with redundant wordlines.

16. (Currently Amended) The method of claim 10, wherein said incrementing, decrementing or incrementing and decrementing values of a test parameter until a minimum or maximum value of said test parameter is reached comprises ~~a linear or~~ binary process.

17. (Original) The method of claim 10, wherein said test parameter is the minimum specified operating voltage of said memory array.

18. (Original) The method of claim 10, wherein said memory array comprises static random access memory cells or dynamic random access memory cells.

19. (Original) The method of claim 10, wherein said memory array is an embedded memory array.

20. (Currently Amended) The method of claim 10, wherein step (c) further includes, before said standard memory testing, removing from said set of tests, any test that tests a parameter that is the same as said test parameter selected in step (b).

21. (New) The method of claim 1, wherein said incrementing, decrementing or incrementing and decrementing values of said test parameter until a minimum or maximum value of said test parameter is reached comprises a linear-process.

22. (New) the method of claim 1, further including:

before performing said set of standard memory tests, reserving said second number of said total number of fuses.

23. (New) The method of claim 1, further including:

terminating schmoo memory testing when a current value of said test parameter requires more than said second number of said total number of fuses for use in repairing said memory array to operate at said current value of said parameter.

24. (New) The method of claim 10, wherein said incrementing, decrementing or incrementing and decrementing values of said test parameter until a minimum or maximum value of said test parameter is reached comprises a linear process.

25. The method of claim 10, further including:

before performing said set of standard memory tests, reserving said second number of said total number of fuses.

26. The method of claim 10, further including:

terminating schmoo memory testing when a current value of said test parameter requires more than said second number of said total number of fuses for use in repairing said memory array to operate at said current value of said parameter